UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,646	10/10/2003	Roy D. Cideciyan	HSJ920030151US1 (HITG.047	1233

			EXAMINER
7590	02/08/2005		MERCEDES, DISMERY E

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ART UNIT	PAPER NUMBER
2651	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/683,646	CIDECIYAN ET AL.
	Examiner	Art Unit
	Dismery E Mercedes	2651

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*10 October 2003*</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,16-19,28-32 and 44* is/are rejected.

7)☒ Claim(s) *5-15,20-27,33-43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some *   c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date <u>*10/10/2003*</u>.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1.   The information disclosure statement (IDS) submitted on 10/10/2003 is in compliance with

the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being

considered by the examiner.

Drawings

2.   The drawings are objected to because: it is not clear whether FIG.3 is prior art or if is part of

an embodiment of the present invention. It is requested that the applicant clarifies such confusion.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office

action to avoid abandonment of the application. Any amended replacement drawing sheet should

include all of the figures appearing on the immediate prior version of the sheet, even if only one

figure is being amended. The figure or figure number of an amended drawing should not be labeled

as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from

the replacement sheet, and where necessary, the remaining figures must be renumbered and

appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the

remaining figures. Each drawing sheet submitted after the filing date of an application must be

labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR

1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and

informed of any required corrective action in the next Office action. The objection to the drawings

will not be held in abeyance.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   Claims 1,2,16-17,28,44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed

et al. (US 5,961,658) in view of Krishnapura et al. (US 6,717,461 B2).

As to Claims 1 & 44, Reed et al. discloses a read channel (col.4, line 28), a viterbi decoder for

decoding a received data stream to produce an estimated sequence representing decoded data bits

(col.4, lines 36-37); and a sequence selection stage for analyzing error events and selecting a

sequence based upon the analysis of the error events (col.4, lines 38-43 and as depicted in fig.9); the

sequence selection stage and the Viterbi decoder each include at least one threshold (as depicted in

Table 2, col.7, lines 33-35; col.10, lines 21-26).

Reed et al. fails to particularly disclose at least one threshold of the sequence selection stage

and the Viterbi decoder is dynamically biased to improve detection reliability in the presence of data

dependent noise.

However, Krishnapura et al. discloses a technique for implementing a dynamic biased circuit,

such as the one depicted in FIG.10e. Therefore, it would have been obvious to one of ordinary skill

in the art, at the time of invention to implement a circuit such as the one disclosed by Krishnapura

et al. into the system disclosed by Reed et al., the motivation being because it would provide such

system with the enhanced capability of providing noise reduction for small input signals, thus

showing the external linearity and syllabic companding of the dynamically biased filter (col.14, lines 1-5 of Krishnapura et al.).

As to Claim 2, in the obvious combination as stated above, Reed et al. further discloses an equalizer for receiving a readback signal and producing a desired target response at the Viterbi decoder (as depicted in FIG.5, "74", col.10, lines 8-9).

As to Claim 16, Reed et al. discloses a memory for storing data (as depicted in Fig.9, "188", col.13, line 64); and a processor configured for decoding a received data stream to produce an estimated sequence representing decoded data bits, for analyzing error events and for selecting a sequence based upon the analysis of the error events (col.4, lines 36-37; col.4, lines 38-43 and as depicted in fig.9); wherein the processor includes at least one threshold (as depicted in Table 2, col.7, lines 33-35; col.10, lines 21-26). Reed et al. fails to particularly disclose at least one threshold is dynamically biased to improve detection reliability in the presence of data dependent noise.

However, Krishnapura et al. discloses a technique for implementing a dynamic biased circuit, such as the one depicted in FIG.10e. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention to implement a circuit such as the one disclosed by Krishnapura et al. into the system disclosed by Reed et al., the motivation being because it would provide such system with the enhanced capability of providing noise reduction for small input signals, thus showing the external linearity and syllabic companding of the dynamically biased filter (col.14, lines 1-5 of Krishnapura et al.).

As to Claim 17, Reed et al. further discloses an equalizer for receiving a readback signal and producing a desired equalized target response at the Viterbi decoder (as depicted in FIG.5, "74", col.10, lines 8-9).

As to Claim 28, Reed et al. discloses a processor configured for decoding a received data stream to produce an estimated sequence representing decoded data bits (col.4, lines 36-37), analyzing error events and selecting a sequence based upon the analysis of the error events (col.4, lines 38-43 and as depicted in fig.9) based upon a chosen threshold (as depicted in Table 2, col.7, lines 33-35; col.10, lines 21-26). Reed et al. fails to particularly disclose the threshold is dynamically biased to improve detection reliability in the presence of data dependent noise.

However, Krishnapura et al. discloses a technique for implementing a dynamic biased circuit, such as the one depicted in FIG.10e. Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention to implement a circuit such as the one disclosed by Krishnapura et al. into the system disclosed by Reed et al., the motivation being because it would provide such system with the enhanced capability of providing noise reduction for small input signals, thus showing the external linearity and syllabic companding of the dynamically biased filter (col.14, lines 1-5 of Krishnapura et al.).

5.   Claims 3,4,18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed et al. (US 5,961,658) in view of Krishnapura et al. (US 6,717,461 B2), further in view of Lee et al. (US 6,148,431).

The combination of Reed et al. and Krishnapura et al. discloses the read channel as claimed in base claim 1 (supra), however, they fail to particularly disclose a branch metric generator for generating distance metrics for a received data stream; a plurality of adders for adding the distance metric for each possible branch to a previously accumulated path metric to produce a revised path metric for each branch; at least one comparator for comparing the revised path metric for a plurality of branches; and a selector for selecting a path metric for a path having a smallest path metric.

However, Lee et al. discloses a branch metric generator for generating distance metrics for a

received data stream (as depicted in FIG.3, "302", col.4, lines 20-21, 26-29); a plurality of adders for

adding the distance metric for each possible branch to a previously accumulated path metric to

produce a revised path metric for each branch (as depicted in FiG.6-7, col.6, line 60); at least one

comparator for comparing the revised path metric for a plurality of branches (as depicted in FiG.6-

7, col.6, line 60); and a selector for selecting a path metric for a path having a smallest path metric

(as depicted in FiG.6-7, col.6, line 60; col.6, line 66-col.7, line 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the

invention to implement an ACS circuit as disclosed by Lee et al. into the read channel disclosed by

Reed et al. and Krishnapura et al, the motivation being, because it would provide the read channel

with the enhanced capability proving an updated or current state metric value in a parallel operation

(col.3, lines 4-15, and col.4, lines 4-5 of Lee et al.).

As to claim 4, in the obvious combination Reed et al. and Krishnapura et al further discloses

a read channel wherein the at least one comparator includes a threshold for making a bias

adjustment to improve detection reliability in the presence of data dependent noise, as discussed in

base claim 1, supra.

As to Claim 18, the combination of Reed et al. and Krishnapura et al. disclosed the system as

claimed in base claim 16, but fails to particularly disclose the processor is further configured for

adding the distance metric for each possible branch to a previously accumulated path metric to

produce a revised path metric for each branch, for comparing the revised path metric for a plurality

of branches and for selecting a path metric for a path having a smallest path metric.

However, Lee et al. discloses adding the distance metric for each possible branch to a

previously accumulated path metric to produce a revised path metric for each branch (as depicted in

FiG.6-7, col.6, line 60 & col.6, line 66-col.7), for comparing the revised path metric for a plurality of branches and for selecting a path metric for a path having a smallest path metric (as depicted in FiG.6-7, col.6, lines 9-23, line 60 and col.6, line 66-col.7, line 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement an ACS circuit as disclosed by Lee et al. into the read channel disclosed by Reed et al. and Krishnapura et al, the motivation being, because it would provide the read channel with the enhanced capability proving an updated or current state metric value in a parallel operation (col.3, lines 4-15, and col.4, lines 4-5 of Lee et al.).

As to claim 19, in the obvious combination Reed et al. and Krishnapura et al further discloses a read channel of claim wherein the at least one comparator includes a threshold for making a bias adjustment to improve detection reliability in the presence of data dependent noise, as discussed in base claim 16, supra.

6.   Claim 29, 30 are rejected as being unpatentable over Sawaguchi et al. (US 2002/0040462), in view of Reed et al. (US 5,961,658), further in view of Krishnapura et al. (US 6,717,461 B2).

Sawaguchi et al. discloses a data storage system comprising at least one storage medium for storing data thereon (as depicted in FiG.5 & 7; page 11, ¶0101); a motor for moving the at least one storage medium (as depicted in FIG.7, "305"; page 11, ¶0102); a transducer, operatively coupled to the at least one storage medium, for reading and writing data on the at least one storage medium (FIG.7, "303"; page 11, ¶0101); an actuator, coupled to the transducer, for translating the transducer relative to the at least one storage medium (FIG.7, "304"; page 11, ¶0101).

Sawaguchi fails to particularly disclose a read channel for processing a data stream received via the transducer, the read channel further comprising: a Viterbi decoder for decoding a received

data stream to produce an estimated sequence representing decoded data bits; and a sequence

selection stage for analyzing error events and selecting a sequence based upon the analysis of the

error events; wherein the sequence selection stage and the Viterbi decoder each include at least one

threshold, and wherein at least one of the threshold of the sequence selection stage and the Viterbi

decoder is dynamically biased to improve detection reliability in the presence of data dependent

noise.

However, Reed et al. discloses a read channel (col.4, line 28), a viterbi decoder for decoding

a received data stream to produce an estimated sequence representing decoded data bits (col.4, lines

36-37); and a sequence selection stage for analyzing error events and selecting a sequence based

upon the analysis of the error events (col.4, lines 38-43 and as depicted in fig.9); the sequence

selection stage and the Viterbi decoder each include at least one threshold (as depicted in Table 2,

col.7, lines 33-35; col.10, lines 21-26).

Reed et al. fails to particularly disclose at least one threshold of the sequence selection stage

and the Viterbi decoder is dynamically biased to improve detection reliability in the presence of data

dependent noise.

However, Krishnapura et al. discloses a technique for implementing a dynamic biased circuit,

such as the one depicted in FIG.10e. Therefore, it would have been obvious to one of ordinary skill

in the art, at the time of invention to implement a circuit such as the one disclosed by Krishnapura

et al. into the system disclosed by Reed et al., the motivation being because it would provide such

system with the enhanced capability of providing noise reduction for small input signals, thus

showing the external linearity and syllabic companding of the dynamically biased filter (col.14, lines

1-5 of Krishnapura et al.).

Therefore it would have been obvious to one of ordinary skill in the art, at the time of the invention, to implement a read channel as disclosed by Reed et al. and Krishnapura et al. into the data storage system of Sawaguchi et al., the motivation being because it would provide the data storage system with the enhanced capability of providing a performance gain and reduce the probability of errors (col.4, lines 20-25 of Reed et al.).

As to Claim 30, in the obvious combination as stated above, Reed et al. further discloses an equalizer for receiving a readback signal and producing a desired target response at the Viterbi decoder (as depicted in FIG.5, "74", col.10, lines 8-9).

7.   Claim 31,32 are rejected as being unpatentable over Sawaguchi et al. (US 2002/0040462), in view of Reed et al. (US 5,961,658), further in view of Krishnapura et al. (US 6,717,461 B2).

The combination of Sawaguchi et al., Reed et al. and Krishnapura et al. discloses the read channel as claimed in base claim 29 (supra), however, they fail to particularly disclose a branch metric generator for generating distance metrics for a received data stream; a plurality of adders for adding the distance metric for each possible branch to a previously accumulated path metric to produce a revised path metric for each branch; at least one comparator for comparing the revised path metric for a plurality of branches; and a selector for selecting a path metric for a path having a smallest path metric.

However, Lee et al. discloses a branch metric generator for generating distance metrics for a received data stream (as depicted in FIG.3, "302", col.4, lines 20-21, 26-29); a plurality of adders for adding the distance metric for each possible branch to a previously accumulated path metric to produce a revised path metric for each branch (as depicted in FiG.6-7, col.6, line 60); at least one comparator for comparing the revised path metric for a plurality of branches (as depicted in FiG.6-

7, col.6, line 60); and a selector for selecting a path metric for a path having a smallest path metric

(as depicted in FiG.6-7, col.6, line 60; col.6, line 66-col.7, line 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the

invention to implement an ACS circuit as disclosed by Lee et al. into the read channel disclosed by

Reed et al. and Krishnapura et al, the motivation being, because it would provide the read channel

with the enhanced capability proving an updated or current state metric value in a parallel operation

(col.3, lines 4-15, and col.4, lines 4-5 of Lee et al.).

As to claim 32, in the obvious combination Reed et al. and Krishnapura et al further

discloses a read channel of claim wherein the at least one comparator includes a threshold for

making a bias adjustment to improve detection reliability in the presence of data dependent noise, as

discussed in base claim 29, supra.

Allowable Subject Matter

8.   Claims *5-15,20-27,33-43* are objected to as being dependent upon a rejected base claim, but

would be allowable if rewritten in independent form including all of the limitations of the base claim

and any intervening claims.

Conclusion

9.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure:

- Ashley et al. (US 2004/0032683 A1) discloses method and apparatus for calibrating data-

  dependent noise prediction.

- Glover (US 6,101,227) discloses a detector and method for detecting defects in the magnetic

  media of a mass storage system.

- Bush et al. (US, 6,158,027) discloses an enhanced noise-predictive maximum likelihood (NPML) data detection method and apparatus for direct access storage device (DASD).

- Leung et al. (US 6,546,518) discloses a detector error suppression circuit and method.

- Yamaguchi et al. (EP 0871170 A2) discloses information reproducing apparatus and reproducing method.

- Feyh et al. (US 6,396,254 B1) discloses a read channel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dismery E Mercedes whose telephone number is 703-306-4082. The examiner can normally be reached on Monday - Friday, from 9:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on 703-305-4040. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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